CLAIMS

What is claimed is:

1. An integrated circuit structure comprising:

a chip level test access port (TAP) controller having a chip-level TAP instruction register; and

a plurality of embedded TAPs connected to said chip level TAP,

said embedded TAPs having instruction register lengths that differ from said chip-level TAP instruction register, and

wherein said chip level TAP includes a flexible length instruction register adapted to accommodate different length instruction registers of said embedded TAPs.

2. The integrated circuit structure in claim 1, wherein said flexible length instruction register is longer than the longest embedded TAP instruction register.

3. The integrated circuit structure in claim 2, wherein additional bits that make said flexible length instruction register longer than the longest embedded TAP instruction register comprises bits that are adapted to choose the active segments of said flexible length instruction register.

4. The integrated circuit structure in claim 1, wherein said flexible length instruction register comprises:

a first instruction register segment having the same length as the shortest embedded TAP instruction register; and

a second instruction register segment having a length equal to the difference between said shortest embedded tap instruction register and a larger embedded tapped instruction register.

5. The integrated circuit structure in claim 1, wherein said flexible length instruction register comprises:

a first instruction register segment having the same length as the shortest embedded TAP instruction register; and

additional instruction registers segments having incremental lengths equal to the difference between the previous shorter embedded tap instruction register and the next largest embedded TAP instruction register.

6. The integrated circuit structure in claim 5, further comprising a plurality of multiplexors connected to said additional instruction register segments, wherein said multiplexors are adapted to selectively include incremental ones of said additional instruction register segments to incrementally match the difference in length between longer embedded TAPs instruction registers and the chip-level TAP instruction register length.

7. The integrated circuit structure in claim 5, wherein the active length of said flexible length instruction register comprises the selected ones of said additional instruction registers segments.

8. The integrated circuit structure in claim 1, wherein said flexible length instruction register appears as a fixed length instruction register to users connecting to said chip level TAP.

9. The integrated circuit structure in claim 1, further comprising selection logic adapted to actively connect only a single embedded TAP at a time to said chip level TAP.

10. An integrated circuit structure comprising:

a chip level test access port (TAP) controller having a chip-level TAP instruction register; and

a plurality of embedded TAPs connected to said chip level TAP,

said embedded TAPs having instruction register lengths that differ from said chip level TAP instruction register, and at least some of the embedded TAP instruction register lengths may differ from each other,

wherein said chip level TAP includes a flexible length instruction register adapted to accommodate different length instruction registers of said embedded TAPs, and

wherein said flexible length instruction register comprises:

a first instruction register segment having the same length as the shortest embedded TAP instruction register; and

a second instruction register segment having a length equal to the difference between said shortest embedded tap instruction register and a larger embedded tapped instruction register.

11. The integrated circuit structure in claim 10, wherein said flexible length instruction register is longer than the longest embedded TAP instruction register.

12. The integrated circuit structure in claim 11, wherein additional bits that make said flexible length instruction register longer than the longest embedded TAP instruction register comprises bits that are adapted to choose the active length of said flexible length instruction register.

13. The integrated circuit structure in claim 10, wherein said flexible length instruction register appears as a fixed length instruction register to users connecting to said chip level TAP.

14. The integrated circuit structure in claim 10, further comprising selection logic adapted to actively connect only a single embedded TAP at a time to said chip level TAP.

15. An integrated circuit structure comprising:

a chip level test access port (TAP) controller having a chip-level TAP instruction register; and

a plurality of embedded TAPs connected to said chip level TAP,

said embedded TAPs having instruction register lengths that differ from said chip level TAP instruction register, and at least some of the embedded TAP instruction register lengths may

differ from each other,

wherein said chip level TAP includes a flexible length instruction register adapted to accommodate different length instruction registers of said embedded TAPs, and

wherein said flexible length instruction register comprises:

a first instruction register segment having the same length as the shortest embedded TAP instruction register; and

additional instruction register segments having incremental lengths equal to the difference between the previous shorter embedded tap instruction register and the next largest embedded tapped instruction register.

16. The integrated circuit structure in claim 15, wherein said flexible length instruction register is longer than the longest embedded TAP instruction register.

17. The integrated circuit structure in claim 16, wherein additional bits that make said flexible length instruction register longer than the longest embedded TAP instruction register comprises bits that are adapted to choose the active length of said flexible length instruction register.

18. The integrated circuit structure in claim 15, further comprising a plurality of multiplexors connected to said additional instruction registers segments, wherein said multiplexors are adapted to selectively include incremental ones of said additional instruction registers segments to incrementally match the difference in length between longer embedded TAPs instruction registers and the chip-level TAP instruction register length.

19. The integrated circuit structure in claim 15, wherein the active length of said flexible length instruction register comprises the selected ones of said additional instruction register segments.

20. The integrated circuit structure in claim 15, wherein said flexible length instruction

register appears as a fixed length instruction register to users connecting to said chip level TAP.

21. The integrated circuit structure in claim 15, further comprising selection logic adapted to actively connect only a single embedded TAP at a time to said chip level TAP.

22. An integrated circuit structure comprising:

a chip level test access port (TAP) controller; and

a plurality of embedded TAPs connected to said chip level TAP,

said embedded TAPs having instruction register lengths that differ from said chip level TAP instruction register, and at least some of the embedded TAP instruction register lengths may differ from each other,

wherein said chip level TAP includes a flexible length instruction register adapted to accommodate different length instruction registers of said embedded TAPs,

wherein said flexible length instruction register is longer than the longest embedded TAP instruction register, and

wherein additional bits that make said flexible length instruction register longer than the longest embedded TAP instruction register comprises bits that are adapted to choose the active length of said flexible length instruction register.

23. The integrated circuit structure in claim 22, wherein said flexible length instruction register comprises:

a first instruction register segment having the same length as the shortest embedded TAP instruction register; and

a second instruction register segment having a length equal to the difference between said shortest embedded tap instruction register and a larger embedded tapped instruction register.

24. The integrated circuit structure in claim 22, wherein said flexible length instruction register comprises:

a first instruction register segment having the same length as the shortest embedded TAP

instruction register; and

additional instruction registers segments having incremental lengths equal to the difference between the previous shorter embedded tap instruction register and the next largest embedded tapped instruction register.

25. The integrated circuit structure in claim 24, further comprising a plurality of multiplexors connected to said additional instruction registers, wherein said multiplexors are adapted to selectively include incremental ones of said additional instruction registers segments to incrementally match the length of longer embedded TAPs instruction registers.

26. The integrated circuit structure in claim 24, wherein the active length of said flexible length instruction register comprises the selected ones of said additional instruction register segments.

27. The integrated circuit structure in claim 22, wherein said flexible length instruction register appears as a fixed length instruction register to users connecting to said chip level TAP.

28. The integrated circuit structure in claim 22, further comprising selection logic adapted to actively connect only a single embedded TAP at a time to said chip level TAP.

29. The integrated circuit structure in claim 22, wherein said embedded TAPs comprise serially connected TAPs.

30. The integrated circuit structure in claim 22, wherein the number of said embedded TAPs is unlimited.